AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended) A method for programming a single bit nonvolatile memory cell integrated on a metal-dielectric-semiconductor technology chip, the memory cell comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a control gate electrode and a dielectric stack, the control gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein the method for programming comprises:

applying electrical ground to the source;

applying a first voltage having a first polarity to the drain;

applying a second voltage of the first polarity to the control gate electrode; and

applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate,

wherein the first, second and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers from the drain of the memory cell, at least some of the hot carriers being (i) generated by a secondary impact ionization mechanism~~, the hot carriers~~ (ii) ~~being~~ injected into the at least one charge storage dielectric layer and (iii) stored on the at least one charge storage dielectric layer ~~from a drain side of the memory cell~~.

Claim 2 (original) The method of claim 1, wherein absolute values of each of the first, second and third voltages are 5 V or less.

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Claim 3 (original) The method of claim 1, wherein a difference of absolute values of any two voltages of the first, second and third voltages is 1.5 V or less.

Claim 4 (original) The method of claim 1, wherein an effective gate-to-substrate voltage applied by the second and third voltages is at least 4 V.

Claim 5 (original) The method of claim 4, wherein absolute values of each of the second third voltages are 5 V or less.

Claim 6 (original) The method of claim 1, wherein the charge storage dielectric layer is positioned between two oxide layers.

Claim 7 (original) The method of claim 1, wherein the charge storage dielectric layer comprises nitride.

Claims 8-11 (canceled)

Claim 12 (currently amended) A memory circuit comprising:

an array of single bit nonvolatile memory cells, each of the memory cells comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a control gate electrode and a dielectric stack, the control gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer;

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peripheral circuitry, the peripheral circuitry coupled with the memory cell such that programming of each memory cell is effected using voltages having absolute values of 5 V or ~~less~~ less,

wherein the memory cells are programmed as a result of injection of hot carriers from the drain of the memory cell, at least some of the hot carriers being (i) generated by a secondary impact ionization mechanism, (ii) injected into the at least one charge storage dielectric layer and (iii) stored on the at least one charge storage dielectric layer.

13. (original) The memory circuit of claim 12, wherein the peripheral circuitry comprises circuitry for generating an on-chip voltage, having an absolute value of 5V or less.

14. (currently amended) A memory circuit, comprising:

an array of single bit nonvolatile memory cells organized in columns, wherein each of the memory cells comprises a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein:

adjacent memory cells in each column of the memory circuit have one of their sources and their drains in common;

the sources of the memory cells in each column of the memory circuit are coupled with the same bitline, the bitline running parallel with the column;

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the drains of the memory cells in each column of the memory circuit are coupled with a respective ~~wordline~~ program line, the ~~wordline~~ program line running perpendicular to the column; and

the gates of the memory cells in each column of the memory circuit are coupled with a respective ~~program~~ word line, the ~~program~~ word line running perpendicular to the column,

wherein programming a memory cell of the memory circuit comprises:

applying electrical ground to a first bitline;

applying a first voltage having a first polarity to a wordline;

applying a second voltage of the first polarity to a program line;

applying a third voltage, having a second polarity opposite to the first polarity to the semiconductor substrate; and

applying a fourth voltage of the first polarity to all other bitlines of the memory circuit.

Claim 15 (canceled)

Claim 16 (previously presented) The memory circuit of claim 14, wherein absolute values of each of the first, second and third voltages are 5 V or less, and an absolute value of the fourth voltage is 2 V or less.

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